FABRICATION AND OPERATION OF A SELF-CONTAINED BUBBLE DOMAIN MEMORY CHIP*

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ABSTRACT

This paper describes the fabrication and operation of a 52-bit bubble domain memory chip designed to test the concept of on-chip magnetic decoding. Access to one of the chip's four shift registers for the read, write, and clear functions is by means of bubble domain decoders utilizing the interaction between a conductor line and a bubble. All other functions are performed by a permalloy overlay driven by an external rotating field. The metallurgy consists of 200 Å evaporated permalloy for magnetoresistive sensors, 4000 Å electroplated permalloy for propagation etc., and 6000 Å electroplated copper for control lines.

INTRODUCTION

The concept of a self-contained magnetic bubble domain memory chip was set forth in a recent paper by Chang, et al.[1]. The chip contains a number of individual shift register, and is designed to be used in a memory which provides random access to blocks of information which are then read out serially. However, rather than using coincident block access[2] to select a chip and a common communication channel[3] to transfer information into and out of a chip, these functions are both performed using an on-chip magnetic decoder made up of logic gates utilizing the interaction between a bubble domain and a current-carrying conductor. The chief advantage of this approach is the simplicity of the resulting memory organization, as further discussed in a companion paper[4]. Here, we describe the design, fabrication, and operation of such a memory chip.

DESIGN

The design chosen to test this concept is shown in block-diagram form in Fig. 1. It consists of four shift registers and all the control functions necessary to write into, read out, and clear any one of the four shift registers. Each shift register has a built-in write decoder and read decoder section. Since the emphasis was on testing the control functions, the storage capacity of each register is small (only 13 bits). The same layout to be described here can provide access to four much longer shift registers, and in a full-scale chip, between 90% and 95% of the total area is available for storage.

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Methods for generation, propagation, and annihilation of bubbles with a permalloy overlay and a rotating in-plane field have already been described[5,6]. Magnetoresistive sensors for bubble domains have also been reported[7,8] The write, clear, read decoder, and write decoder functions make use of a current-controlled switch which is shown in Fig. 2. This switch allows a small control current to select one of two alternate paths in the permalloy overlay for the bubble domain. A bubble B entering the switch from the right will emerge from the upper port if the current I is positive, and from the lower port if I is negative. The complete chip layout is shown in Fig. 3.

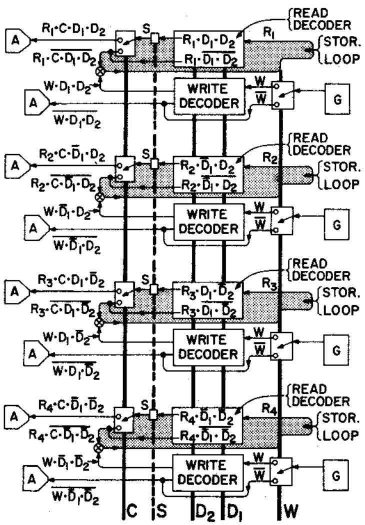

Fig. 1. Block diagram of the memory chip's operation. (G--generator, A--annihilator, S--sensor, W--write control line, D_1, D_2--decode control lines, C--clear control line, R_1, R_2, R_3, R_4--information stored in register 1, 2, 3, or 4)

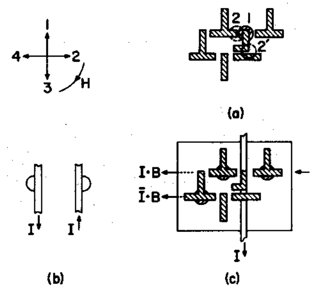

Fig. 2. The basic switch.

a.) In the absence of control current, it is uncertain whether the bubble will move from position 1 to 2 or 2'.

b.) Effect on bubble position of current in a stripline.

c.) Combining the permalloy and conductor patterns as shown results in the "single-pole, double throw" switch whose Boolean representation is shown here. (The current is on between field positions 1 and 2.)

Since logic as well as storage are being accomplished on the chip, it is useful to represent the switch in Boolean algebra. The switch may be viewed as a two-output logic element operating on the two binary inputs B and I. B will be considered 1 when a bubble is present and 0 when a bubble is absent; I will be considered 1 for positive current and 0 for negative current. Then the output at the upper port is the Boolean "And" function (B•I), whereas the other